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SURVEY OF STUCK-AT FAULT MODELS IN VLSI TESTING: METHODS, TOOLS, AND OPTIMIZATION STRATEGIES

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Abstract: The addition of continuous improvement of the Very Large-Scale Integration (VLSI) technology has led to improvements in digital systems through the provision of extra performance, reduced size, and energy efficiency. But, due to increased complexity of integration and a decrease in technology nodes, fault detection and diagnosis in VLSI circuits have become a difficult problem. This review paper gives an extensive description of stuck-at fault models, extensions thereof and contemporary testing techniques of VLSI systems. It describes the basic fault modeling principle, single and multiple stuck-at fault models, and the current innovations of simulation methods, memory BIST routines and implementations of test sets of validation. In addition, the concept of artificial intelligence (AI) and machine learning (ML) integration in fault detection, low-power optimization, and hardware security is highly examined. The limits of traditional fault testing and the opportunities of AI-driven frameworks to solve the issues of scalability and diagnostic efficiency are explicitly identified in the comparative analysis of the state-of-the-art methodologies. The purpose of this survey is to fill in the gap between the past models and future fault-tolerant VlSI systems as well as establish future research directions in the field of fault modeling and test automation.

Keywords: VLSI testing, stuck-at fault model, Fault Diagnosis; Memory BIST; Delay Testing; Machine Learning in VLSI; Combinational circuits

1 INTRODUCTION

Modern electrical power systems are complex, extensive, and interconnected systems over a large geographical area. These systems are made up of generators, transformers, trans- mission lines, and loads as well as other protective equipment such as relays and circuit breakers[1]. Also, they operate as balanced 3-phase AC power systems such as when they are in their normal conditions, the magnitude of both currents and voltages are equally distributed between each phase[2]. Optimization technique in the field of engineering is a powerful tool to utilize the resources in an efficient way as well as to reduce the environmental impact of a process. Application of optimization process helps us achieve the most favourable operating conditions. Any engineering or research discipline involving design, maintenance and manufacturing requires certain technical decisions to be taken at different stages[3]. The outcome of taking these decisions is to maximize the profit with minimum utilization of resources. Optimization search has a good significance in appearing a weakness of the simulated model and guiding the software for best executing.

The VLSI design has undergone several technology nodes by introducing more computational density as well as energy efficiency. Nonetheless, due to the physical constraints of Moore Law, conventional scaling cannot be relied upon to be able to satisfy the growing demands in speed, power efficiency, and area optimization[4]. Fault detection is a considerably more significant but more difficult process in contemporary electronic design due to the Very Large-Scale Integration (VLSI) circuits. With integrated circuits (ICs) becoming increasingly more functional and larger in size, it is becoming much more challenging to ensure their reliability[5]. Conventional fault detection methods, including Automatic Test Pat-tern Generation (ATPG) and Built-In Self-Test (BIST) are showing increasing weaknesses in scalability, computation power, and accuracy. Both the industry and academia have become more and more interested in this area due to the need to have high-performance and reliable systems[6]. Many delay fault models, and a vast variety of test methodologies, have been suggested to address this increased complexity of timing verification over the last 20 years.

Modern VLSI systems will likely be capable of performing a variety of complex tasks-artificial intelligence and high-speed communications as well as quantum computing and real-time analytics. This has resulted in a new way of conceptualizing, designing, and manufacturing chips[7]. The designers are now faced with the challenge of having to strike a balance between various goals: low power, high performance, thermal management, reliability and design time. Delay testing has proved to be one of the best solutions to find out timing-related faults in present-day VLSI circuits[8]. Digital circuits frequently contain stuck-at faults, which are bridging faults, missing gate faults, cross-point faults and cell faults and can be studied in terms of two behavioural models. The first is **online testing**, where fault detection is performed during the circuit's normal operation[9]. It provides built-in self-testable environment over design methodology and circuit modification for the detection of fault models in terms of single and multiple bit faults. The test set generation is followed by numerous numbers of methodologies for respective fault models in MCT based circuits.

1.1 Structure of the paper

This paper is organized as follows: Section 2. Fundamentals of fault modelling in VLSI. Section 3A new model for multiple Section 4. Testing Strategies for Stuck-at Fault Detection. Section 5 Literature of review of recent studies, Section 6 Shown in conclusion of study and future insights.

2 FUNDAMENTALS OF FAULT MODELING IN VLSI

Fault models at the logic level have been generated from the structure of logic circuits made of transistors. These fault models, which constitute the main contribution of this paper, will enable the future development and precise evaluation of new defect-and fault-tolerant architectures for Nano electronic systems[10]. Injection of the fault models can be a powerful technique to carry out the evaluation of the system, while doing it at a manageable cost. Wear-out (aging) and transient faults are also important issues that must be deeply analyzed in future research.

2.1 Circuit Models

Circuit models give reduced electrical models that are employed to understand the behaviour of a system, forecast its performance and facilitate effective design and optimization[11]. In order to make the performance analysis easier, a practical digital circuit of different logic gates like AND gate, OR gate, etc. is chosen. In addition, the methods acquired to test these circuits are generally enough to similar circuits that consist of modified logic gates like AND gate with some simple modifications and so on. The delay of this logic gates used is presumed to be identical as shown in Figure 1.

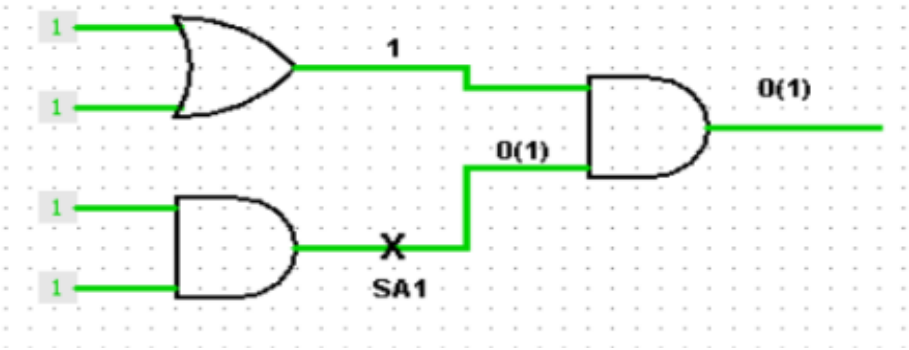
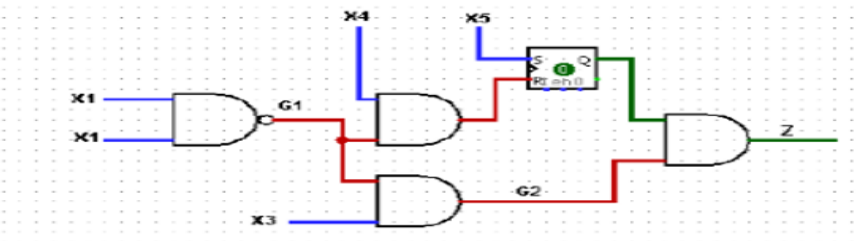


Figure 1: Testing Circuit

2.2 Problem model

The objective is to create a sample model or to consider the flaw as recurring for each fault in the overview of a defect and to construct a test of collection of measuring defects. Further, the stuck-at-fault phenomenon occurs only in the case of hardware[12]; however, it is not possible to create a combinational circuit or any such physical model in software and test the faults, generate the test vectors. The software model will give the output as per the characteristics of used combinational gates or any elements and the given test inputs[13]. If the selection line is 0, stuck-at-zero fault will propagate through the circuit and if 1 is given then stuck-at one fault will propagate through the circuit. Besides, for rest of the inputs of selection line, the fault free output will be obtained. Simulation of the given circuit in viva do will allow the test vectors of the faulty outputs to be actualized and counted. The circuit model can also be used for realizing the multiple-stuck-at-fault. The realized model for single stuck- stuck-at fault is presented in the Figure 2.



	X1	X2	X3	X4`	X5
T1	1	0	0	1	0
T2	1	0	0	0	0
T3	0	1	0	0	0
T4	0	1	1	0	0

Figure 2: Single Stuck at Fault Model Circuit

2.3 Serial simulation

This is the most basic and simple algorithm to simulate Faults[14]. The circuit is first modelled in true value mode, and all the vectors and primary outputs are saved to a file. Then, on-by-one simulation of all faulty circuits is performed. This is done on the true-valued simulator, by setting up the circuit with desired fault. The performance of faulty circuit increasingly contradicts the saved true values as the simulation goes forward. Once the correlation shows the identification of the desired fault, the simulation of the fault circuit if turned off. It simulates all faults serially. Logic faults influence the status of logic signal. The normal state can be represented as a set of {0, 1, X, Z} and a fault can transform a true value into another.

Table 1 shows the differentiations between circuit models, problem models and serial simulation techniques are revealed in a comparative approach of major fault modelling methods in VLSI. Their purpose, their main concepts, their failure-handling abilities, their uses, their advantages and their shortcomings have been summarized in the table and that gives a clear idea on how each of the methods plays a role in the process of effective fault identification and verification in digital circuit.

TABLE I. COMPARATIVE ANALYSIS OF FUNDAMENTAL FAULT MODELING APPROACHES IN VLSI

Aspect	Circuit Models	Problem Model	Serial Simulation
Purpose	It offers simplified circuit representations and uses them to study the behavior and performance of circuits	Produces a software model, which is used to model recurrent faults and produces test vectors	Sequentially tests the faults by finding the difference between faulty results and stored true values
Core Concept	Thras gastronomically analyzes with practical digital circuits (AND, OR, etc.) which have the same gate delay	Models stuck-at faults (0 or 1) in software because real hardware modeling is not possible	Simulation Runs the simulation in true-value mode then compensates according to each fault to identify deviations
Fault Handling	Helps the performance analysis and can be expanded to the fault-tolerant architecture testing	Simulates single and multiple faults by sticking at faults with simulation tools such as Vivado	Identifies logic errors by simulating signals as the signals of [0,1, X, Z] and corrupted results
Application	Applications for the evaluation of nanoelectronic systems and optimization as well as verification of modified logic gate designs	Helps produce and tally test vectors of faulty outputs on a basis of selection-line behavior	Detects faults through step-by-step simulation of all possible faults until a mismatch is obtained
Key Advantage	Helps to simplify the study of the complicated behaviour of circuits at moderate cost	Is able to sense several stuck-at faults without a need to physically construct the circuit	Uncomplicated, straightforward algorithm which can be applied directly out of the true-value simulation
Limitation	Makes the assumption of the (possibly not real) hardware behavior of equal delay of all gates	restricted to the quality of the software model; is not capable of generating all the effects of real hardware	Slow computationally since errors are modeled individually

3 MODELING AND DIAGNOSIS OF MULTIPLE STUCK-AT FAULTS IN VLSI CIRCUITS

A multiple stuck at fault of multiplicity n can be modelled as a single stuck at fault by using at most n+3 gates. Consider the circuit in the Figure 3. To convert the multiple stuck at fault in to a single stuck at fault model the following steps have to be performed:

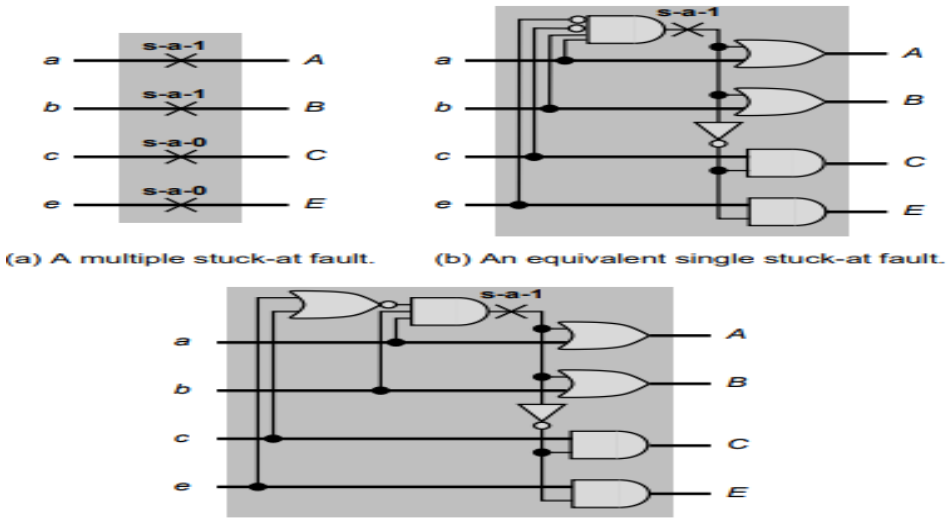


Figure 3: A Mmodel for a Multiple Stuck-At Fault.

- **Step 1:** A two-input gate is inserted in each faulty line. An AND gate is inserted in a line with stuck at 0 fault and an OR gate is inserted in a line with a stuck at 1 fault. These are called In-line gates.
- **Step 2:** n input AND gate is fed with the second input of the In-line gates. The In-line OR gates are fed by the output of this AND gate and the In-line AND gates are fed by an inverter. This gate has the n inputs which are based on the s-a-1 fault lines.

The model (b) contains a single stuck-at fault. It consists of two types of

- **Type 1:** In-line gates: In every faulty line, a two-input gate is placed. The controlling input signal state for this gate is the same as the value at which the line is stuck. Thus, an AND (OR) gate is inserted in a line that is stuck-at-0 (1). When the fault on a line is not activated, the in-line gate forces the correct value on it.
- **Type 2:** Fault gate: This is an input AND gate that feeds all in-line gates either directly if the in-line gate is OR type, or through an inverter if it is AND type. All the s- a -1 lines are directly used to give the fault gate inputs and all s- a -0 lines are inverted to give the fault gate inputs. A single s-a-1 fault is modeled at the output of this gate.

3.1 Multiple faulted for sequential Circuits

Faults for Sequential Circuits the model have shown in Figure 4 can also be used for the multiple faults in the combinational logic of any sequential circuit[15]. The fault equivalence conditions 1 and 2 still hold regardless of sequential elements in the circuit. Any multi-stuck multiple faults of multiplicity n are still modellable.

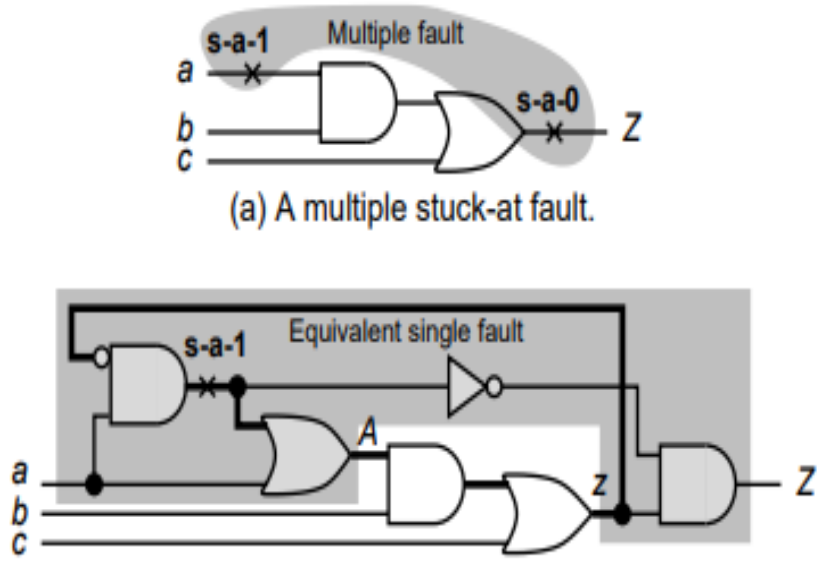


Figure 4: Illustration of Non-Functional Feedback.

With at most n+3 gates. The modelling structure may create non-functional feedback within the combinational circuit logic but the seemingly asynchronous behaviour will never be activated.

3.2 Fault Simulation and the Matching Algorithm

The diagnosis procedure uses sequential circuit fault simulation of single stuck-at faults. Simulation is performed on a candidate list of faults to determine their outputs responses[16]. This is then compared to the failing response, and each candidate fault is given a score based on a matching algorithm. All out-put pins on which the failing device produces a faulty response for the particular vector are considered. For each of these out-put pins, if a candidate fault produces a faulty response, then its score is incremented by 2. If it is potentially detected on any of these outputs, that are its output is an X, then its score is incremented by 1. The candidate faults are ranked according to the scores.

3.3 Tools in Stuck Fault Analysis

Stuck-fault analysis tools These are tools created to model, inject, and analyze stuck-at-0 and stuck-at-1 faults in digital circuits. These tools usually comprise of fault simulators, test pattern generators and circuit modelling environments which assist in determining the propagation of faults through logic gates[17]. Software such as Modalism and Viv ado, and other ATPG tools are used to generate test vectors automatically, mismatch faulty loads with fault-free loads, and fault coverage. A combination of these tools can be used to effectively detect, diagnose and validate faults in both sequential and combinational circuits.

4 TESTING STRATEGIES FOR STUCK-AT FAULT DETECTION

Diagnosis of a logic circuit is implemented by performing some tests and observing the resultant outputs. A test is an input combination that defines the desired response that a faultless circuit ought to give. When the response that is observed is not the one that is expected, then there is a Fault in the circuit[18]. Testing on the gate level is to ensure that every logic gate in the circuit is working correctly and the interconnections are sound. Henceforth, also deal with stuck-at faults only unless mentioned otherwise. If only a single stuck-at fault is assumed to be present in the circuit under test, then the problem is to construct a test set that will detect the fault by utilizing only the inputs and the outputs of the circuit.

4.1 Procedures used before for testing

Different methods are used for testing stuck at fault in combinational circuits like Adding buffer to each port of RTL circuits the more procedures are as given below:

- Firstly, test bench is developed and the simulation is done on a good circuit and then on each of the faulty circuits using any simulator.
- The outputs obtained in each case of the faulty circuits are compared with the output of the good circuits to determine where fault actually occurred the fault list is tabulated.
- The ratio of the numbers of RTL faults detected to the total number of RTL faults gives the RTL fault coverage.

4.2 Fault Testing

The proposed memory BIST algorithm is used for fault testing. It states the memory failures and the information preparing of the fail state to the repair block.

4.3 BIST Algorithm for Fault Testing

To deliver high-grade SoC products, the SoC manufacturer needs high fault coverage. Therefore, most manufacturers try to implement a sophisticated memory BIST algorithm to reach reasonable percent fault coverage. Most memory BIST schemes are based on the marching algorithm to test the embedded memories and get significant fault coverage. Generally, a complex March algorithm can detect fault types, such as stuck-at fault, address decoder fault, transition faults, and some coupling faults[19]. The current product's increased chip density and technology result in new fault types in the SoC, such as stuck-open fault and neighbourhood pattern sensitive faults (NPSFs). The designer needs to provide the algorithm carefully with these advancements in technology.

4.4 Implementation of Validation Test sets

Validation test sets are implemented by gathering controller behaviours/actions derived by some known test sequences and subsequently applying the same behaviours to make justification and propagation in the analysis simpler. This is followed by a heuristic technique that can be used to determine the controller behaviours that are compatible with precomputed test vectors, which only requires one time through the CDFG and is highly precise with very few test-generation runs. Lastly, the generation is done at the RTL level with prespecified controller behaviours and the generation time saved greatly and fault simulation is augmented to establish factions of activation-detection time and to detect compatible faults economic.

- **Controller Behaviour Extraction:** The scheme first derives the controller behaviours from validation test sequences and reuses them for simplifying justification/propagation analysis corresponding to precompiled test vectors/responses of data path RTL modules.

- **Heuristic-Based Compatibility Identification:** The identification of controller behaviours that are consistent with a preliminary set of precomputed test vectors/responses is performed by heuristic. It requires only a single pass through the CDFG corresponding to a validation test sequence and is accurate, resulting in a small number of test generation runs.
- **RTL-Level Test Generation Optimization:** Generation of tests is generated at RTL and the controller behaviour is specified in advance thus leading to very small test generation times. Identification of compatible controller behaviours consisting of Augmented Fault Simulation to Derive Activation-Detection Time Frame Pair and Analysis of Requirements to Identify Compatible Faults.

5 LITERATURE REVIEW

The literature demonstrate that sophisticated AI- and heuristic-based methods significantly improve fault diagnosis, power efficiency, and reliability of the system in VLSI design. But there are issues of scaling these methods, controlling computational overhead and verifying them in various hardware settings.

Hundekari et al.(2025) have shown AI and ML techniques have dramatically influenced rapid developments in low-power VLSI design with fast advancements in device simulations and power optimization strategies. Now AI-based simulation tools are applied to the accurate simulation of power consumption, the enhancement of thermal analysis, and the acceleration of design cycles with the identification of unproductive areas and the optimization of energy use. And leakage current minimization with respect to a sustainable VLSI design Introduction of AI in VLSI simulation enables the enhancement of power efficiency while maintaining sustainability outcomes by optimizing energy usage and cost reduction in terms of computation[20].

Higami et al. (2024) have shown that although most of the diagnosis methods have targeted single stuck-at faults, multiple faults also need to be addressed because methods for diagnosing single stuck-at faults do not cover some of the multiple faults. And also, diagnosis methods for a class of multiple faults are proposed, namely double. After the candidate faults are reduced, fault simulation is conducted for a faulty circuit assuming that the candidate double fault consists of a candidate stuck-at fault and a transition fault obtained from the reduced lists in the earlier step[21].

Dwibedi et al. (2024) shown that in Very Large-Scale Integration (VLSI) design circuit's power dissipation is another crucial requirement that needs to be minimized, especially with increasing growth in the need for power aware electronic systems. And a new generally applicable met heuristic optimization approach utilizing heuristic algorithms as well as machine-enforced models is proposed to for reducing, both dynamic and the steady-state power consumption in VLSI circuits[22].

Lu (2023) have shown that Computer security is becoming more and more important as more aspects of our life rely on information technology. The fundamental building block of information technology is semiconductor. Semiconductor enables Very Large-Scale Integrated (VLSI) Circuits which power the digital infrastructure. This presentation examines the challenges and opportunities of security from the point of view of VLSI design and technology. We first explain why security in general and hardware security in particular is challenging[23].

Higami et al. (2022) described a method which neither needs to perform fault simulation nor it needs to store fault dictionaries in deducing candidate faults. The output responses of a circuit under diagnosis are applied to a trained neural network, and candidate faults are obtained as a result. And also investigated the generation of data that are used to train the neural network. The effectiveness of the proposed method is shown by the experimental results for benchmark circuits[24].

Ishii and Namba (2022) provided an error-tolerant method of deep neural network (DNN) inference using field-programmable gate arrays (FPGAs) over Stuck-at Faults. And achieved a recognition rate of 99.7% for the error-free case by eliminating outliers using a threshold calculated from the median and deviation for the parameters and computing them as 0[25].

Table 2 highlights the research highlights in VLSI since it includes fault diagnosis, power optimization, and hardware security. Although the papers demonstrate higher efficiency and accuracy in diagnosing diseases with the help of AI and heuristic techniques, such aspects as scalability and computation cost remain hard to resolve, so further research is directed at more powerful and efficient VLSI implementations.

TABLE II. SUMMARY OF RECENT STUDIES ON VLSI FAULT ANALYSIS, POWER OPTIMIZATION, AND SECURITY

Reference	Study on	Approach	Key Findings	Challenges / Limitations	Future Directions
Hundekari et al. (2025)	Low-power VLSI design based on AI	Application of AI/ML simulation models in power model, thermal model and efficiency optimization	AI enhances the design iteration, removes leakage to achieve sustainable VLSI, and refines the power estimation	Uses intensive computing power and powerful data sets	Build lighter AI and make design automation even more sustainable
Higami et al. (2024)	Multiple stuck-at faults diagnosis	Simulated faults and candidate lists were proposed to diagnose the double faults	Current techniques identify single faults; their approach can identify double faults, which are complicated	The diagnosis of multiple faults adds to the complexity of computations	Expand the list of types of faults diagnostics and increase scalability

Dwibedi et al. (2024)	Reduction of power dissipation in VLSI	Metaheuristic optimization using heuristics and machine learning	Considerable dynamic and static power saving in VLSI circuits	All types of circuits may not be generalized by heuristic models	Increase flexibility of optimization process and implement deep-learning systems
Lu (2023)	VLSI design security threats	Hardware security topics of semiconductor-based system analysis	Sheds light on the growing threats and vulnerabilities of the semiconductor-based digital systems	Hardware security is complex and challenging since it is subject to changing attack surface	DevCreate new design level security and robust architectures
Higami et al. (2022)	Fault diagnosis based on a neural-network	Neural network to determine candidate faults without fault dictionaries or simulation	NN is able to detect stuck faults and minimizes diagnostic overhead	TQuality of training has a direct influence on accuracy	Enhance NN learning example and investigate hybrid diagnostic models
Ishii & Namba (2022)	Fault-tolerant DNN inference on FPGAs	Error-tolerant FPGA-based DNN approach eliminating outlier parameters	Achieved 99.7% recognition accuracy even under stuck-at faults	Handling severe fault conditions may reduce accuracy	Develop more robust DNN-FPGA architectures for safety-critical systems

6 CONCLUSION AND FUTURE WORK

VLSI testing landscape is still changing with the increasing complexity, performance requirement, and reliability expectation of the modern circuits. This review looked at basic aspects of fault modelling, such as stuck-at faults, multi-fault, situations, and delay-based testing as well as well-known simulation strategies. As much as the conventional methods like ATPG and BIST are still vital, they are not able to keep up with the growing design complexity and fault behaviour types. In order to overcome these drawbacks, new methods have embraced improved modelling systems, memory-based BIST violation and AI-based diagnosis systems. The application of machine learning, neural networks and heuristic algorithms has demonstrated high potential in enhancing test coverage, reducing the fault detection time, and enhancing flexibility in complex architectures. These contemporary solutions are becoming important to the realization of efficient, accurate, and scalable test solutions as VLSI systems are progressing toward greater integration and into heterogeneous configurations.

Future research must focus on the scalable and adaptive fault detection methods with the ability to address the complexity of advanced VLSI systems, such as 3D ICs and heterogeneous SoCs, need to be prioritised in future studies. In addition to single stuck-at models, testing should deal with transition, delay, and intermittent faults with the help of a hybrid diagnostic. Also, AI integration needs to focus on explainable, energy-saving approaches to provide transparency, reliability, and scalability of the next-generation testing systems to industrial levels.

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